What is claimed is:

1. A semiconductor device comprising:

a first element formation region in which a device of a first conductivity type is formed;

a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed;

a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type;

a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type;

a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region containing said second conductivity type impurity, having one end connected to an end of said second gate electrode,

having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes.

2. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are physically connected to each other by a semiconductor layer.

3. A semiconductor device as set forth in claim 1, wherein the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

4. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second gate electrodes.

5. A semiconductor device as set forth in claim 1, wherein said first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

6. A semiconductor device as set forth in claim 1, wherein said element isolation region is buried in a trench formed a boundary between said first and second conductive type of element formation regions in a

semiconductor substrate.

7. A semiconductor device as set forth in claim 1, wherein said element isolation region isolates first and second element formation regions comprised of semiconductor layers formed on an insulation layer.

8. A semiconductor device as set forth in claim 7, wherein said element isolation region is buried in a trench formed in said semiconductor layers.

9. A semiconductor device as set forth in claim 2, wherein:

said semiconductor layer is formed by polycrystalline silicon and

said first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

10. A semiconductor device as set forth in claim 2, wherein the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

11. A semiconductor device as set forth in claim 1, wherein:

the widths of said first and second impurity

storage regions are equal to the gate length of said first and second gate electrodes and

the lengths of said first and second impurity storage regions are longer than said gate length.